REMARKS

The Office Action of August 25, 2004, has been received and reviewed.

Claims 1-39 and 41-67 are currently pending in the above-referenced application. Of these, claims 14-16, 27-30, 34-36, 41, and 48-67 have been withdrawn from consideration. Claims 1-13, 17-26, 31-33, 37-39, and 42-44 stand rejected.

Reconsideration of the above-referenced application is respectfully requested.

Information Disclosure Statement

Please note that a Supplemental Information Disclosure Statement was filed in the above-referenced application on January 27, 2004, but that the undersigned attorney has not yet received any indication that the references cited in the Supplemental Information Disclosure Statement have been considered in the above-referenced application. It is respectfully requested that the references cited in the Supplemental Information Disclosure Statement of January 27, 2004, be considered and made of record in the above-referenced application and that an initialed copy of the Form PTO/SB/08A that accompanied that Supplemental Information Disclosure Statement be returned to the undersigned attorney as evidence of such consideration.

Rejections Under 35 U.S.C. § 112, First Paragraph

Claims 1-13, 17-26, 31-33, 37-39, and 42-44 stand rejected under 35 U.S.C. § 112, second paragraph, for purportedly being indefinite.

Specifically, independent claim 1 was apparently rejected because "adjacent semiconductor" lacked antecedent basis. Independent claim 1, as amended, no longer includes the objected-to language, and complies with the definiteness requirement of the second paragraph of 35 U.S.C. § 112.

Claims 2-13, 17, and 18 were merely rejected for depending from claim 1.

Independent claim 19 was rejected because the Examiner did not understand the structure being recited. Office Action of August 25, 2004, pages 2 and 3. In particular, the Examiner asserted that the recitation that, "prior to securing an intermediate conductive element to any of the bond pads," the nonconfluent spacer layer "protrude[es] from the active surface [of a first

semiconductor device] substantially [the same] distance the active surface of the first semiconductor device is to be spaced apart from the back side of a second semiconductor device . . ."

Extraneous language has been removed from independent claim 19, broadening the scope thereof while clarifying the same. It is clear from the language of independent claim 19 that it is directed a semiconductor device assembly which includes a first semiconductor device and a nonconfluent spacer layer.

By reciting that the nonconfluent spacer layer protrudes from an active surface of the first semiconductor device substantially the same distance that the back side of a second semiconductor device is to be spaced apart from the active surface of the first semiconductor device, it is clear that the nonconfluent spacer layer may be secured to the active surface of the first semiconductor device prior to placement of a second semiconductor device thereover.

Further, by reciting that the nonconfluent spacer layer is secured to the active surface of the first semiconductor device "prior to securing an intermediate conductive element to any of the bond pads" of the first semiconductor device, independent claim 19 clearly indicates that the assembly may include a nonconfluent spacer before the first semiconductor device is electrically connected (by way of intermediate conductive elements, such as bond wires), to another electronic component. In view of the foregoing, it is respectfully submitted that the scope of independent claim 19 is sufficiently clear to comply with the definiteness requirement of 35 U.S.C. § 112, second paragraph.

Of course, a semiconductor device assembly that includes intermediate conductive elements or another semiconductor die may also fall within the scope of independent claim 19.

Claims 20-26, 33, and 42-44 were merely rejected for depending directly or indirectly from claim 19.

For these reasons, withdrawal of the 35 U.S.C. § 112, second paragraph, rejections of claims 1-10, 17, 19-26, 33, and 42-44 is respectfully requested.

Rejections Under 35 U.S.C. § 102(e)

Claims 1-10, 13, 17, 19-26, 32, 33, 37-39 and 42-44 stand rejected under 35 U.S.C. § 102.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single reference which qualifies as prior art under 35 U.S.C. § 102. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Foster

Claims 1-10, 17, 19-26, 33, and 42-44 stand rejected under 35 U.S.C. § 102(e) for being drawn to subject matter which is purportedly anticipated by the disclosure of U.S. Patent 6,552,416 to Foster (hereinafter "Foster").

Foster describes a variety of multichip modules that include tape 32, die attach paste 33, and inner-lead traces 21 between stacked dies 30 and 31. *See, e.g.,* FIG. 8; col. 4, lines 50-57; col. 5, lines 16-23. In particular, the multichip module shown in FIG. 8 of Shim includes a lower die 31 with centrally located bond pads, a first layer of die attach paste 33 on regions of the active surface of the lower die 31, which secures inner-lead traces 21 to the active surface of the lower die 31, tape 32 over the inner-lead traces 21, and a second layer of die attach paste 33 securing the tape 32 to the back side of another, upper semiconductor die 30. *Id.*

It is clear that, while the combined thicknesses of the first layer of die attach paste 33, the inner-lead traces 21, the tape 32, and the second layer of die attach paste 33 may be substantially the same as the distance the lower die 31 and an upper die 30 are to be spaced apart from one another, col. 4, lines 63-67, of Foster that bond wires 35 must be secured to the bond pads of the lower die 31 *before* the second layer of die attach paste 33 is placed over the inner-lead traces 21.

Independent claim 1, as amended and presented herein, recites a semiconductor device that includes a semiconductor die and a dielectric spacer layer that protrudes substantially a predetermined distance from a surface of a semiconductor die before an intermediate conductive element is secured to a bond pad of the semiconductor die. The predetermined distance

accommodates a height of at least one intermediate conductive element between the semiconductor die and an adjacent semiconductor die.

Foster lacks any express or inherent description that the first layer of die attach paste 33, the inner-lead traces 21, the tape 32, and the second layer of die attach paste 33, the combined thicknesses of all of which are necessary to accommodate the height of an intermediate conductive element (*e.g.*, bond wire 35), are all positioned over lower die 31 before an intermediate conductive element (*e.g.*, bond wire 35) is secured to a bond pad of the lower die 31. To the contrary, Foster states that the second layer of die attach paste 33 is not added until after bond wires 35 are secured to the bond pads of the lower die 31. Col. 4, lines 63-67.

Moreover, the series of layers between the dice 30 and 31 of Foster include electrically conductive inner-lead traces 21. Since the inner-lead traces 21 contribute to the overall thickness of the series of layers, the series of layers cannot be characterized as "dielectric," as required by independent claim 1.

Therefore, under 35 U.S.C. § 102(e), the subject matter recited in amended independent claim 1 is allowable over that disclosed in Foster.

Each of claims 2-10 and 17 is allowable, among other reasons, for depending either directly or indirectly from claim 1, which is allowable.

Claim 6 is additionally allowable because Foster does not expressly or inherently describe that the predetermined distance that the multi-layered spacing elements thereof protrudes from the surface of the lower semiconductor die 31 is the same as or less than the distance the bond wires 35 protrude above the surface of the lower semiconductor die 31. Rather, the description of Foster is limited to a series of layers that protrude from the surface of a lower die 31 a distance that exceeds the height that a bond wire 35 protrudes from the surface of the lower die 31.

Claim 9 is further allowable since Foster lacks any express or inherent description that the multi-layered spacing elements thereof may include randomly arranged features.

Independent claim 19 is directed to a semiconductor device assembly that includes a first semiconductor device and a nonconfluent spacer layer. The nonconfluent spacer layer includes dielectric material secured to the active surface of the first semiconductor device. The

nonconfluent spacer layer protrudes from the active surface substantially a same distance that the active surface of the first semiconductor device is to be spaced apart from a back side of a second semiconductor device, even before an intermediate conductive element is secured to any of the bond pads of the first semiconductor device.

Again, Foster lacks any express or inherent description that the first layer of die attach paste 33, the inner-lead traces 21, the tape 32, and the second layer of die attach paste 33 are all positioned over lower die 31 before an intermediate conductive element (*e.g.,* bond wire 35) is secured to a bond pad of the lower die 31. Notably, the combined thicknesses of this series of layers is necessary to accommodate the height of an intermediate conductive element (*e.g.,* bond wire 35) protruding from the lower die 31. Instead, Foster discloses that the second layer of die attach paste 33 is not added until after bond wires 35 are secured to the bond pads of the lower die 31. Col. 4, lines 63-67.

As such, it is respectfully submitted that, under 35 U.S.C. § 102(e), independent claim 19 is directed to subject matter which is allowable over that described in Foster.

Claims 20-26, 33, and 42-44 are each allowable, among other reasons, for depending either directly or indirectly from claim 19, which is allowable.

Claim 26 is additionally allowable because Foster does not expressly or inherently describe that the predetermined distance that the multi-layered spacing elements thereof protrudes from the surface of the lower semiconductor die 31 is the same as or less than the distance the bond wires 35 protrude above the surface of the lower semiconductor die 31.

Shim

Claims 1-10, 13, 17, 19-26, 32, 33, 37-39 and 42-44 are rejected under 35 U.S.C. § 102(e) for reciting subject matter which is allegedly anticipated by the subject matter described in U.S. Patent 6,531,784 to Shim et al. (hereinafter "Shim").

Shim discloses elongated spacer strips 50A, 50B. FIGs. 4-6; col. 4, lines 33-38. The spacer strips 50A, 50B of Shim are formed from insulative material. Col. 4, lines 50-53. Apparently, the spacer strips 50A, 50B of Shim are preformed, as the teachings of Shim are

limited to attachment or mounting (*e.g.*, with adhesive) thereof to a top surface of a semiconductor die 14. Col. 4, lines 56-60; col. 5, line 19; col. 5, lines 32-37; col. 5, lines 62-66.

Spacer strips 50A, 50B do not protrude from the top surface of semiconductor die 14 substantially the same distance that semiconductor die 14 is to be spaced apart from another semiconductor die 16. Rather, as shown in FIGS. 3, 7, 8, and 9 of Shim, once bond wires or other intermediate conductive elements are secured to the bond pads of semiconductor die 14 and to corresponding terminals of a substrate upon which semiconductor die 12 is positioned, an additional adhesive 44 (*see also,* col. 5, lines 10-14) or spacer strip 50C (*see also,* col. 6, lines 6-19) is required to space the second semiconductor die 16 the predetermined distance apart from the active surface of the first semiconductor die 14.

Shim includes no express or inherent description of a semiconductor device that includes a dielectric spacer layer that protrudes from a surface of a semiconductor die a predetermined distance that the semiconductor die is to be spaced apart from another semiconductor die *before at least one intermediate conductive element is secured to a bond pad of the semiconductor die*, as is required by amended independent claim 1. Instead, the description of Shim is limited to spacer strips 50A, 50B that protrude from the surface of a semiconductor die 14 only a portion of the distance the semiconductor die 14 is to be spaced apart from another semiconductor die 16.

Therefore, Shim does not anticipate each and every element of amended independent claim 1, as would be required to maintain the 35 U.S.C. § 102(e) rejection of amended independent claim 1.

Claims 2-10, 13, and 17 are each allowable, among other reasons, for depending either directly or indirectly from claim 1, which is allowable.

Claim 6 is additionally allowable because Shim does not expressly or inherently describe that the predetermined distance that the spacer strips 50A, 50B thereof protrudes from the surface of the lower semiconductor die 14 is the same as or less than the distance the bond wires or other intermediate conductive elements protrude above the surface of the lower semiconductor die 14.

Claim 9 is further allowable since Shim lacks any express or inherent description that the spacer strips 50A, 50B thereof may include randomly arranged features.

With respect to the subject matter recited in amended independent claim 19, Shim lacks any express or inherent description of a semiconductor device assembly that includes a first semiconductor device with a nonconfluent spacer layer protruding from an active surface thereof substantially a predetermined distance the active surface is to be spaced apart from a back side of the second semiconductor device *before an intermediate conductive element*, such as a bond wire, *is secured to any of the bond pads at the active surface of the first semiconductor device.* Rather, the spacers of Shim are not provided with their full heights, which are equal to the distances that semiconductor dice 14 and 16 are spaced apart from one another, until after intermediate conductive elements are secured to the bond pads of the lower semiconductor die 14.

Therefore, under 35 U.S.C. § 102(e), amended independent claim 19 is directed to subject matter which is allowable over the subject matter described in Shim.

Each of claims 20-26, 32, 33, 37-39, and 42-44 is allowable, among other reasons, for depending either directly or indirectly from claim 19, which is allowable.

Claim 26 is additionally allowable because Shim neither expressly nor inherently describes that the predetermined distance that the spacer strips 50A, 50B thereof protrudes from the surface of the lower semiconductor die 14 is the same as or less than the distance that bond wires or other intermediate conductive elements protrude above the surface of the lower semiconductor die 14.

In view of the foregoing, withdrawal of the 35 U.S.C. § 102(e) rejections of claims 1-10, 13, 17, 19-26, 32, 33, 37-39, and 42-44 is respectfully requested.

Rejections Under 35 U.S.C. § 103(a)

Shim in View of Smith

Claims 11 and 12 are rejected under 35 U.S.C. § 103(a) for being drawn to subject matter which is assertedly unpatentable over the teachings of Shim, in view of teachings from U.S. Patent 6,049,370 to Smith, Jr., et al. (hereinafter "Smith".

Claims 11 and 12 are allowable, among other reasons, for depending from claim 1, which is allowable.

Shim in View of Blanton.

Claims 18 and 31 stand rejected under 35 U.S.C. § 103(a) for reciting subject matter which is purportedly unpatentable over the subject matter taught in Shim, in view of the teachings of U.S. Patent 5,220,200 to Blanton (hereinafter "Blanton").

Claim 18 is allowable, among other reasons, for depending from claim 1, which is allowable.

Claim 31 is allowable, among other reasons, for depending from claim 19, which is allowable.

Foster in View of Mueller

Claims 11, 13 and 32 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 6,552,416 to Foster in view of U.S. Patent 6,316,786 to Mueller et al. Applicant respectfully traverse this rejection, as hereinafter set forth.

Claims 11 and 13 are both allowable, among other reasons, for depending directly from claim 1, which is allowable.

Claim 32 is allowable, among other reasons, for depending directly from claim 19, which is allowable.

In view of the foregoing, it is respectfully requested that the 35 U.S.C. § 103(a) rejections of claims 11-13, 18, 31, and 32 be withdrawn.

ELECTION OF SPECIES REQUIREMENT

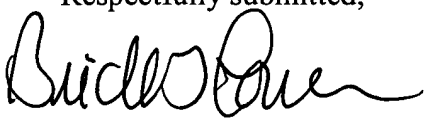
It is respectfully submitted that independent claim 1 remains generic to all of the species of invention that were identified in the Election of Species Requirement in the above-referenced application. In view of the allowability of these claims, claims 14-16, 27-30, 34-36, 41,

and 45-67, which have been withdrawn from consideration, should also be considered and allowed. M.P.E.P. § 806.04(d).

CONCLUSION

It is respectfully submitted that each of claims 1-39 and 41-67 is allowable. An early notice of the allowability of each of these claims is respectfully solicited, as is an indication that the above-referenced application has been passed for issuance. If any issues preventing allowance of the above-referenced application remain which might be resolved by way of a telephone conference, the Office is kindly invited to contact the undersigned attorney.

Respectfully submitted,



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Date: October 28, 2004

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